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CONTACT

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

Circuits and Systems

DISTINGUISHED LECTURER PROGRAM

System Level Design of Low Power Wireless Sensor Networks for Biomedical Applications

Prof. Dinesh K. Bhatia
University of Texas at Dallas
Thursday 02 August 3:30 pm
ASB 10900 - Presentation Studio, SFU

Wireless sensor networks (WSN) will become prevalent in many applications that relate to ubiquitous computing. Integrating a large scale system based on WSN is a challenging task that requires efficient management of hardware as well as software resources. Building a robust and reliable system is a must requirement for using WSN in biomedical applications like tele-health and health monitoring. This talks presents system level issues that must be accounted for building a large scale low power network. The talk is illustrated using the construction of a large health monitoring system. Also, as is evidenced by recent industry trends, this talk will highlight how various companies are positioning themselves to exploit this technology.

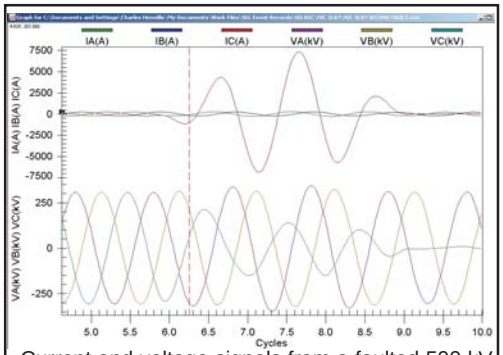
Speaker: Dinesh Bhatia is on the faculty of electrical engineering department at The University of Texas at Dallas. He directs research activities within the Embedded and Adaptive Computing group and is also a member of Center for Integrated Circuits and Systems at the University of Texas at Dallas. He received MS and a Ph.D. in Computer Science from the University of Texas at Dallas. His research interests include all aspects of reconfigurable and adaptive computing, architecture and CAD for field programmable gate arrays (FPGAs), physical design automation of VLSI Systems, biomedical electronics and systems, medical devices, natural energy scavenging and, applications of wireless sensor networks. His recent work on wireless sensor networks operating on scavenged energy is gaining importance in health care applications involving tele-medicine and remote health monitoring as well as in problems related to monitoring and alleviation of wood logging in forests. He has extensive experience in building large scale embedded and reconfigurable systems. Some of these activities include principal designer and investigator for RACE and NEBULA systems for Wright Laboratories of USAF, principal investigator for DARPA funded REACT program, Co-PI on AFRL funded SPARCs program and several more. He has published extensively in leading journals and conferences and continues to serve on program committees of several conferences. He is a senior member of IEEE, Computer Society, Circuits and Systems Society, Eta Kappa Nu, and recently served on the editorial board of IEEE Transactions on COMPUTERs. He is IEEE Circuits and Systems society's distinguished lecturer for 2007.
Website: http://www.ensc.sfu.ca/people/faculty/jiel/ieee/dlp_Bhatia.html
Sponsors: IEEE Circuits and Systems joint Chapter of the Vancouver/Victoria Sections
Info: Chapter Chair Ljiljana Trajkovic ljilja@cs.sfu.ca

Continuing Education

A Practical Approach to Electric Power System Protection

This 36 hour course will be presented over 12 weeks on Wednesday evenings from September to December. It is intended to give practicing electrical engineers an understanding of the fundamentals of protective relaying applied to electric power systems.

Topics to be covered include:
• role of protection in power systems, transducers and protection accessories • short circuit calculations • protection measuring elements (including the principles of digital filtering) • protection of transmission and distribution systems • protection of generators and interconnections to power systems • protection of substation equipment • special protection systems • analysis of real life disturbances
• power system components.



Current and voltage signals from a faulted 500 kV transmission line

In addition to an understanding of the basic principles of power system protection, this course provides an opportunity for engineers to learn about the impact of protection functions on the power system itself. Protective relays provide an important contribution to the security of power systems by minimizing the impact of short circuits and other disturbances that could otherwise lead to cascading and blackouts.

This course will unveil many of the mysteries associated with "the art and science of protective relaying".

The course is planned to be offered from 5:00-8:00 pm on Wednesday evenings starting September 5th, 2007. Course location will be the BC Hydro Office, 6911 Southpoint Drive, Burnaby, BC (Near the Edmonds skytrain station).
The cost of the course will be $700 for IEEE members, and $800 for non members. For registration please contact Jose Marti, jrms@ece.ubc.ca
For information on the course content, please contact Charlie Henville chenville@dccnet.com

The course instructors have many years of experience of power system protection.

Mukesh Nagpal received the Ph.D. and M.Sc. degrees in electrical engineering from the University of Saskatchewan, Saskatoon, SK, Canada. Currently, he is a Specialist Engineer cum Team Leader with BC Hydro Engineering, Protection and Control Planning Group, Burnaby, BC, Canada. He is also an Adjunct Professor with the University of British Columbia and was a Part-Time Instructor with the British Columbia Institute of Technology. He has more than 19 years of experience in electrical consulting, utility research, and power system protection.
Dr. Nagpal has written more than 20 technical papers on power system relaying. He has also contributed to numerous ANSI/IEEE sponsored standards or guides on relaying practices.

Charlie Henville, is a specialist in electric power system protection. After a thirty year career with BC Hydro, he retired in 2005 from the position of principal engineer. He now runs his own consulting company in power system protection. Charlie is well experienced in training engineers in power systems.
He is adjunct faculty at the University of Wisconsin and the University of BC, and has presented training courses to working engineers world wide. He is a Fellow of the Institute of Electrical and Electronic Engineers, and a past recipient of APEGBC's President's Award for professional service.


Uncleared short circuit in substation. *(Click photo for 5MB mpg QuickTime footage, about 30 secs.)*

Joint Communications

10 Gigabit Ethernet for High-performance Real-time Embedded Systems

Rob Kraft
AdvancedIO Systems Inc.
Monday 20 August 2007 700-900pm
BCIT Campus Townsquare D
3700 Willingdon Ave, Burnaby

10 Gigabit Ethernet (10GbE) technology, which is still relatively new in the server space, is now emerging in the real-time embedded space, overlapping the emergence of other proprietary and standard system interconnect fabrics such as RapidIO, and PCI Express. What makes 10-Gigabit Ethernet so exciting is that for the first time, the world's most widely understood, deployed, and accepted packet-based communications protocol can address the requirements of the high performance real-time space.

Unfortunately, the act of processing the communication protocol stack at 10 Gigabit rates heavily taxes modern processors and DSPs , leaving them very few, if any, cycles to perform signal processing.

Input/Output (I/O) devices, such as Analog-to-digital converters , could also benefit from using 10GbE as a communications fabric if a 10GbE interface could be effectively 'attached' to them.

In this talk we will discuss key issues when practically implementing 10GbE in high-performance real-time embedded systems. Among them: - the requirement for protocol acceleration or offload - architectural issues when 'attaching' 10GbE to I/O devices - some key system-level benefits of using Field Programmable Gate Arrays (FPGAs) for implementing the 10GbE interfaces and protocol offload To set the context, the talk will begin with an introduction to the high-performance real-time embedded industry, including: - a simplified introduction to the concept of standard buses, fabrics, and form factors like VME, PCI, CompactPCI, PCI-X, PCI Express (PCIe), AdvancedTCA, microTCA, VXS, VPX, RapidIO - standard mezzanine module form factors like PMC and XMC - some applications

Speaker: Rob Kraft is the VP of Marketing at AdvancedIO Systems Inc. He is responsible for ensuring that AdvancedIO's products meet market needs, solve compelling business issues, and achieve recognition in the marketplace. Before joining AdvancedIO, Rob spent over 11 years in systems engineering, technical sales, and product management with Spectrum Signal Processing, AlliedSignal Aerospace, and Alcatel Transport, successfully delivering integrated systems to satisfied customers. Rob enjoys giving presentation and has a strong technical background in the embedded space. He holds a BASc degree in Engineering Science (Electrical) and an MASc in Systems Control Engineering from the University of Toronto, and is a registered Professional Engineer. You may occasionally spot Rob on-stage at one of the stand-up comedy venues around Vancouver - often in front of a very quiet crowd.

Info: Communications Chair Alon Newton anewton@ieee.org

Computer

Medical Embedded Systems

Majid Sarrafzadeh, UCLA
Tuesday 14 August 2007 400-530pm
Electrical & Computer Engineering
2332 Main Mall - Kaiser 2020, UBC (map)

Light-weight embedded systems are now gaining more popularity due to recent technological advances in fabrication of more powerful tiny processors. In particular, the field of pervasive computing and medical monitoring is emerging due to the development of tiny and low-profile computing nodes, mated with sensors and actuators, in close proximity to the human. In distributed embedded systems, often battery-powered, it is critical to extend the system lifetime for each individual node in order to retain the functionality of the entire network for the longest possible time. We will describe an e-optimal polynomial time technique that evenly distributes the communication load over the nodes. This formulation can be exploited to optimize system power consumption or to enhance network reliability. Both power and reliability issues are among the most significant concerns in medical embedded systems.

Speaker: Majid Sarrafzadeh (M'87, SM'92,F'96) received his Ph.D. in 1987 from the University of Illinois at Urbana-Champaign in Electrical and Computer Engineering under the supervision of Professor Franco Preparata. He joined Northwestern University as an Assistant Professor in 1987. In 2000, he joined the Computer Science Department at University of California at Los Angeles (UCLA). His recent research interests lie in the area of Embedded and Reconfigurable Computing, VLSI CAD, and design and analysis of algorithms.

Dr. Sarrafzadeh is a Fellow of IEEE for his contribution to "Theory and Practice of VLSI Design". He has served on the technical program committee of numerous conferences in the area of VLSI Design and CAD, including ICCAD, DAC, EDAC, ISPD, FPGA, and DesignCon. He has served as committee chairs of a number of these conferences. He is on the executive committee/steering committee of several conferences such as ICCAD, ISPD, and ISQED. He was the program committee and the general chair of ICCAD in 2004 and 2005 – the premiere conference in CAD.

Professor Sarrafzadeh has published approximately 350 papers, co-authored 5 books, and is a named inventor on 6 US patents. Dr. Sarrafzadeh is an Associate Editor of ACM Transaction on Design Automation (TODAES) and an Associate Editor of IEEE Transactions on Computers and a number of other journals. Dr. Sarrafzadeh has collaborated with many industries in the past fifteen years including IBM and Motorola and many CAD industries and was the architect of the physical design subsystem of Monterey Design Systems – Synopsys acquired the company. He was a co-founder of Hier Design, Inc. which was acquired by Xilinx in 2004.

Info: Computer Chair Philippe Kruchten pbk@ece.ubc.ca

Vancouver Section members recently elevated to IEEE Senior Member

Ahmed Elneweihi
Ki Cheong Ho
Juri Jatskevich
Mukesh Nagpal
Frank Plumptre
Robert Schober
R. Stewart
Emile Struyk

IEEE UCE/SPAM FILTERING SERVICE TO CHANGE FROM "OPT-IN" TO "OPT-OUT"

To help reduce the increasingly large volume of unsolicited commercial email messages - commonly known as spam - being sent to ieee.org email addresses from outside sources, the IEEE UCE/spam filtering service will be changing from the current "opt-in" policy to an "op-out" policy."

On 20 August 2007, a default spam filtering level, expected to reduce the volume of email sent to ieee.org addresses by 30 percent, will be applied to all IEEE email aliases. It is designed to filter out email that is extremely likely to be UCE/spam. In the past, this filtering service had to be individually activated by each user.

Those who do not wish to have the default spam filtering level applied to their IEEE email alias can select to "opt-out" at https://uce.ieee.org and choose the "No UCE/Spam filtering" option, or select a more aggressive filter level. After choosing this option, click on "Set UCE/Spam Filtering Level" button to save the changes.
If no action is taken by 20 August, the default spam filtering level will be activated. Subscribers can opt-out of the filtering service at any time.

For more details on why the new policy was implemented, how the policy will improve email delivery through internet service providers and the aggressiveness of the service, visit https://uce.ieee.org/opt-out-info.html. Questions can be directed to member-services@ieee.org.

IEEE MENTORING CONNECTION™ SEEKS NEW MEMBERS

The IEEE Mentoring Connection is seeking additional "online" mentors to help guide younger professionals in career planning and professional development. Mentor participation is open to all higher grade IEEE members.

Currently, a mentor in Florida is partnered with members in Hong Kong and China, and a mentor in Ireland is partnered with a member in Saudi Arabia. Other mentors in the United States are currently matched with individuals in Japan, Nigeria and India. 833 mentees and 371 mentors have registered for the program to date.

Potential mentors are asked to review the time and effort commitment to the program necessary to ensure a successful mentoring partnership. Currently, mentors are asked to dedicate a minimum of two hours a month. Interested members can visit http://www.ieee.org/mentoring for more information on the roles and responsibilities of each mentoring partner, including additional program information and an FAQ page.
Questions? Contact Cathy Downer at c.downer@ieee.org

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Prescreens job seekers with an interactive profile feature to identify the most qualified candidates for your unique requirements
Provides resumes matched to your needs quickly and cost-effectively
Join the hiring managers at more than 3,000 leading corporations - in fields ranging from ASIC design to aerospace and defense system development - that use the IEEE Job Site - http://www.spectrum.ieee.org/jobsite/jump/r7promo.html
If you have any questions, e-mail at employerjobsite@ieee.org <mailto:employerjobsite@ieee.org>.

**** One free post per company referred by an IEEE Member***